## WHAT IS CLAIMED IS:

- 1. A method of testing an electronic device that includes a CPU and at least one memory, comprising the steps of:
  - (a) testing the at least one memory, using the CPU; and
  - (b) testing the CPU.
- 2. The method of claim 1, wherein said testing of the CPU is effected subsequent to said testing of the at least one memory.
  - 3. The method of claim 1, further comprising the step of:
  - (c) loading a testing program into one of said at least one memory, the CPU then testing at least one of said at least one memory by executing said testing program.
  - 4. The method of claim 1, further comprising the step of:
  - (c) storing results of said testing of said at least one memory in one of said at least one memory, by the CPU.
- 5. The method of claim 4, wherein said testing of the CPU includes reading said stored results from said one of said at least one memory.
- 6. The method of claim 1, wherein said testing of said at least one memory is effected during a burn-in of the electronic device.

- 7. A method of testing an electronic device that includes a CPU, a nonvolatile memory and a volatile memory, comprising the steps of:
  - (a) testing at least one of the memories, using the CPU; and
  - (b) testing the CPU.
- 8. The method of claim 7, wherein said testing of the CPU is effected subsequent to said testing of said at least one memory.
  - 9. The method of claim 7, further comprising the step of:
  - (c) loading a testing program into the volatile memory, the CPU then testing at least one of the memories by executing said testing program.
  - 10. The method of claim 9, further comprising the step of:
  - (d) storing said testing program in the nonvolatile memory, said loading of the testing program into the volatile memory then being from the nonvolatile memory.
- 11. The method of claim 10, wherein said loading of the testing program from the nonvolatile memory to the volatile memory is effected by the CPU.
  - 12. The method of claim 7, further comprising the step of:
  - (c) storing results of said testing in the nonvolatile memory, by the CPU.
- 13. The method of claim 12, wherein said testing of the CPU includes reading said stored results from said nonvolatile memory.

- 14. The method of claim 7, further comprising the step of:
- (c) storing a testing program in the nonvolatile memory, the CPU then testing at least one of the memories by executing said testing program directly in said nonvolatile memory.
- 15. The method of claim 14, further comprising the step of:
- (d) storing results of said testing in the nonvolatile memory, by the CPU.
- 16. The method of claim 15, wherein said testing of the CPU includes reading said stored results from said nonvolatile memory.
- 17. The method of claim 7, wherein said testing of at least one of the memories is effected during a burn-in of the electronic device.
- 18. A method of testing a nonvolatile memory that is included in a system-in-package, comprising the steps of:
  - (a) including a CPU in the system-in-package;
  - (b) storing a testing program in the nonvolatile memory; and
  - (c) executing said testing program, by said CPU, in order to test the nonvolatile memory.
  - 19. The method of claim 18, further comprising the step-of:
  - (d) loading said testing program from the nonvolatile memory into a volatile memory, said executing of said testing program then being from said volatile memory.

- 20. The method of claim 19, further comprising the step of:
- (e) including said volatile memory in the system-in-package.
- 21. The method of claim 18, further comprising the step of:
- (d) storing results of said executing in the nonvolatile memory.
- 22. The method of claim 18, wherein said executing is effected during a burn-in of the nonvolatile memory.
  - 23. An electronic device comprising:
  - (a) a nonvolatile memory wherein is stored a first testing program for testing said nonvolatile memory; and
  - (b) a volatile memory, operationally connected to said nonvolatile memory;

and wherein a second program, for testing said volatile memory, is stored in said nonvolatile memory.

- 24. The electronic device of claim 23, wherein said nonvolatile memory and said volatile memory are fabricated as separate respective chips and are packaged together in a common package.
  - 25. The electronic device of claim 24, further comprising:
- (c) a CPU, fabricated on a respective chip, and operationally connected to at least one of said nonvolatile memory and said volatile memory; said CPU being packaged together with said memories in said common package.

- 26. A method of testing a system-in-package that includes a nonvolatile memory and a volatile memory, comprising the steps of:
  - (a) executing a first testing program in order to test the volatile memory; and
  - (b) storing results of said executing in the nonvolatile memory.
  - 27. The method of claim 26, further comprising the steps of:
  - (c) executing a second testing program in order to test the nonvolatile memory; and
  - (d) storing results of said executing of said second testing program in the nonvolatile memory.
- 28. The method of claim 26, wherein said executing is effected during a burn-in of the volatile memory.